Richard C. Walker
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Richard Walker was born in San Rafael, CA, in 1960. He received the B.S. degree in Engineering and Applied Science from the California Institute of Technology in 1982, and an M.S. degree in Computer Science from California State University, Chico, CA in 1992. Rick joined Agilent Laboratories (formerly Hewlett-Packard Laboratories) in 1981, where he is currently a Principal Project Engineer. Since that time, he has worked in the areas of broadband-cable modem design, solid-state laser characterization, linecode design, and gigabit-rate serial data transmission. He holds 15 U.S. patents.

Research

Optical Engines and Optical-Cable Assemblies Capable of Low-Speed And High-Speed Optical Communication

- Patent Full-text available Dec 2015
- Mathieu Charbonneau-Lefort · William Richard Trutna · Richard C. Walker · Michael John Yadlowski

Optical Touch - Screen Systems And Methods Using A Planar Transparent Sheet

- Patent Full-text available Dec 2015
- Jeffrey King · Timothy James Orsley · William Richard Trutna · Richard C. Walker

Robust Optical Touch - Screen Systems And Methods Using A Planar Transparent Sheet

- Patent Full-text available Jun 2015
- Jeffrey King · Dragan Pikula · Richard C. Walker

Integrated circuit for facilitating optical communication between electronic devices

- Patent Full-text available Sep 2014
- Richard C. Walker

Apparatuses, systems, and methods for facilitating optical communication between electronic devices

- Patent Full-text available Mar 2013
- Richard C. Walker

Multi-phase sampling

- Patent Full-text available May 2007
- Richard C. Walker

Coding method for coding packetized serial data with low overhead

- Patent Full-text available May 2006
- Richard C. Walker · Birdy Amrutur · Richard Dugan

Immersive Display System

- Patent Full-text available Mar 2005
- Richard C. Walker · Pierre Mertz · Barclay Tullis
Data communication system with self-test facility

Network monitoring system with built-in monitoring data gathering

Electro-optical material-based grey scale generating method

Multiplexer with channel sectioning, selectively actuated current sources, and common-base amplifiers

Adaptive decoder for skin effect limited signals

Personal viewing device with system for providing identification information to a connected system

Coding method and coder for packetized serial data with low overhead

Decoding method and decoder for 64b/66b coded packetized serial data

Immersive Display System

Designing Bang-Bang PLLs for Clock and Data Recovery in Serial Data Transmission Systems
System and method for efficiently handling an input data stream by utilizing a predictor, look-ahead feature, unified states

Method and system for compensating for defects in a multi-light valve display system

Electro-optic material based display device having analog pixel drivers

64b/66b decoding for packetized serial data

Coding for packetized serial data

Analog pixel drive circuit for an electro-optical material-based display device

Oversampling Rotational Frequency Detector

Fully Integrated High-Speed Interleaved Voltage-Controlled Ring Oscillator

Modulation and Frequency Conversion by Time Sharing

A 2.488 Gb/s Si-bipolar clock and data recovery IC with robust loss of signal detection

SONET 2.488Gb/s transmission and switching systems, network backbones, and video transmission are among the many application areas benefiting from inexpensive and robust clock and data recovery circuits (CDR). Previous commercial solutions have required multiple chips and GaAs processes to perform this function. This 25GHz f<sub>T</sub>/f<sub>T</sub> Si-bipolar chip operates from 2 to 3Gb/s over worst-case process, temperature, and supply voltage.

A 2.488-Gbit/s silicon bipolar clock and data recovery circuit for SONET fiber-optic communications networks
Adjustment-free clock and data recovery for 2.488-Gbit/s SONET applications is provided by a 1.77W, 3.45 x 3.45-mm2 chip implemented in a 25-GHz FET silicon bipolar process. The chip has an on-chip VCO and operates from 2 to 3 Gbits/s over process, voltage, and temperature variations with a single off-chip filter capacitor. For network monitoring, a highly reliable loss-of-signal detector is provided. For good mechanical, thermal...
The design and implementation of a chipset for gigabit/second computer networks

**Article** Full-text available Jul 1992
Richard C. Wa ker
Thesis (M.S.)-California State University, Chico. Includes abstract. Includes bibliographical references (leaves [48]-51).

W. McFarland · Richard C. Walker · C. Stout · C.-S. Yen
A link interface chipset that conforms to the Serial-HIPPI (High-Performance Parallel Interface) specification is presented. The chipset contains all portions of the link interface and link control functions specified in Serial-HIPPI. The simple additional circuitry required to create a complete Serial-HIPPI link using this chipset is detailed. The two-chip set can also serve as a general-purpose link with no additional circuitry. It transfers...

Richard C. Wa ker · J. T. Wu · C. Stout · C.-S. Yen · P. Petruno
The authors report a monolithic transmitter and receiver chip pair which implements a full-duplex virtual ribbon cable interface. For short-distance applications, on-chip equalizer is provided to allow use of coaxial cables rather than a more costly fiber link. The chips require no external frequency-determining elements or user adjustments and operate over a range of 600 to 1500 MHz using an on-chip VCO (voltage-controlled...

**Article** Full-text available Jul 1991 · IEEE Journal on Selected Areas in Communications
Richard C. Wa ker · T. Hornak · C.-S. Yen · Kent H. Springer
The authors designed a set of four ICs to provide encoding, multiplexing, clock extraction/demultiplexing, and decoding for gigabit-rate serial data transmission. These chips form a high bandwidth data link for point-to-point communication. A new line code is implemented that provides DC balance, efficient encoding, framing, and simple clock extraction. Embedded in the code is a fixed transition used by the phase/frequency locke...

**Patent** Full-text available Jun 1991
Crandall · S. R. Hessel · T. Hornak · Richard C. Wa ker

**Patent** Full-text available May 1991
Richard C. Wa ker · H. Braun

**Patent** Full-text available Apr 1991
B. Lal · Richard C. Wa ker

A chipset for gigabit rate data communication [using optical fibres]

A gigabit-rate data link consisting of four custom silicon bipolar chips for transmitting parallel data between elements of a distributed computer system is discussed. A transmission rate of 16 bits in parallel at 50 MHz or with encoding overhead, a serial rate of 1 Gb/s is demonstrated. The link utilizes an encoding scheme that is bandwidth efficient. Unlike other links, the phase/frequency-locked loop also provides frame...