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Drinker Biddle & Reath LLP (Marvell) 191 N. Wacker Drive Chicago, IL 60606			MYERS, ERIC A	
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

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### **DETAILED ACTION**

1. The present application is being examined under the pre-AIA first to invent provisions.
2. This is in response to an amendment filed 12/17/2014.
3. No claims have been amended.
4. No claims have been cancelled.
5. No new claims have been added.
6. Claims 1-20 remain pending in the application.

### ***Response to Arguments***

7. Applicant's arguments filed 12/17/2014 have been fully considered but they are not persuasive.

**Regarding claims 1-20**, Applicant asserts that the rejection of claims including similar elements over Walker and Sakoda was withdrawn during prosecution of U.S. Patent Application No. 11/431,929 ("the '929 Application), which is a grandparent application to this Application.

The Examiner respectfully disagrees with Applicant's assertion. The Examiner notes that the claims of the instant application appear to be broader than the originally filed claims in the '929 Application, which were rejected over Walker in view of Sakoda. The Examiner also notes that the scope of claim 1 in the '929 Application was narrowed in an amendment filed 7/22/2009 in response to the non-final rejection of claim 1 over Walker in view of Sakoda dated 3/17/2009. Amended claim 1 and dependent claims 2-

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9 were then rejected over Walker in view of Ichino, but the rejection of original claims 10-18 over Walker in view of Sakoda was maintained. The final rejection of the '929 Application thus does not contain any indication that a rejection of claims containing the subject matter of the claims of the instant application over Walker in view of Sakoda was withdrawn.

**Regarding claims 1-20**, Applicant argues that the proposed modification would render Walker unsuitable for its intended purpose. Applicant asserts that replacing the two-bit header with a single-bit header would render the communication scheme of Walker vulnerable to single-bit errors in the header. Applicant also asserts that Walker relies on the two-bit header for maintaining a balance of 1's and 0's for a balanced line code in a bit serial transmission and guaranteeing a transition from 1 to 0 and from 0 to 1 for the purposes of clock recovery.

The Examiner respectfully disagrees with Applicant's interpretation of the prior art. The Examiner also notes that Applicant is arguing solely against the Walker reference when the claims were rejected over Walker in view of Sakoda. Applicant cites col. 15, lines 25-45 of Walker as explaining how a two-bit header helps a decoder to detect errors. However, this portion of Walker does not appear to state any requirement for a two bit header, but merely states that master transition errors as large as four bits can be detected in the decoder. Applicant asserts that using a single-bit header would render the communication scheme of Walker vulnerable to single-bit errors in the header, but the cited portion of Walker states that errors as large as four bits can be detected. Such errors may be reasonably interpreted to include single-bit errors. With

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regard to Applicant's assertion that Walker relies on the two-bit header for maintaining a balance of 1's and 0's for a balanced line code in a bit serial transmission and guaranteeing a transition from 1 to 0 and from 0 to 1 for the purposes of clock recovery, the Walker reference does not appear to recite any such reliance. The Walker reference does not appear to state that a two-bit header is required to maintain a balance of 1's and 0's for a balanced line code or for the purposes of clock recovery.

**Regarding claims 1-20**, Applicant argues that Walker teaches away from making the alleged combination of Walker and Sakoda. Applicant asserts that Walker provides specific reasons why a two-bit header should be used at least at col. 7, lines 31-47 and col. 15, lines 26-46.

The Examiner respectfully disagrees with Applicant's interpretation of the prior art. Col. 7, lines 31-47 appears to state that a two-bit header is used, but does not appear to provide any statement or assertion that a two-bit header must be used. Col. 15, lines 26-46 appears to state that although the two bit header may appear to suffer from the disadvantage that a two-bit error can convert the kind of frame defined by the master transition from a frame that lacks the TYPE word to a frame that includes the TYPE word, the decoder can detect master transition errors as large as four bits. This portion of the specification therefore also does not appear to state any strict requirement that a two-bit header is explicitly required. Because the Walker reference does not contain any statements explicitly disclaiming the use of a one-bit header, the Walker reference does not teach away from the combination of Walker and Sakoda.

### ***Double Patenting***

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit <http://www.uspto.gov/forms/>. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled

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out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to <http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp>.

9. Claims **1-20** are rejected on the ground of nonstatutory obviousness-type double patenting over **claims 1-16** of U.S. Patent No. **8,472,478**. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are obvious variations.

In view of the above, it is noted that the instant application is broader than the **Patent 8,472,478**, thus, allowing this would result in an unjustified or improper timewise extension of the “right to exclude” granted by a patent.

10. Claims **1-20** are rejected on the ground of nonstatutory obviousness-type double patenting over claims **1-18** of U.S. Patent No. **7,809,021** since the claims, if allowed, would improperly extend the “right to exclude” already granted in the patent. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are obvious variations.

In view of the above, it is noted that the instant application is broader than the **Patent 7,809,021**, thus, allowing this would result in an unjustified or improper timewise extension of the “right to exclude” granted by a patent.

***Claim Rejections - 35 USC § 103***

11. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. This application currently names joint inventors. In considering patentability of the claims under pre-AIA 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of pre-AIA 35 U.S.C. 103(c) and potential pre-AIA 35 U.S.C. 102(e), (f) or (g) prior art under pre-AIA 35 U.S.C. 103(a).



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14. Claims 1-20 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over **Walker et al. (US 6,718,491)** in view of **Sakoda et al. (US 6,088,345)**.

**As per claim 1**, Walker discloses a method for coding a packet of information words into frames for transmission (see figure 1,64b encoder, see column 4, lines 27-30, 4 lane bus), the method comprising:

receiving blocks of input data, the input data including control words and the packet of information words (see column 7, lines 1-10, composed of information words and control words), the packet having (a) a start preceded by ones of the control words and (b) an ending followed by others of the control words (see figure 2, SOP 131 and EOP 132, see column 7, lines 10-21, the control words in the four lanes the start of the packet indicated by SOP control word S, then information words, followed by EOP control word T), the blocks being smaller than the packet (see column 7, lines 1-10, data received by encoder 100 via the four lanes of the bus, composed of information words and control words, the number of information words in the packet 130 is substantially fewer than the minimum number of information words in an Ethernet packet);

determining whether a block consists exclusively of information words and when the block consists exclusively of information words (see column 9, lines 10-25, a type 1 block composed exclusively of information words) appending to the block a two bit block header having a first sense to form the frame (see column 9, lines 10-25, a type 1 block composed exclusively of information words, composed of a two bit field 01 and the payload field, by encoding);

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when the block does not consist exclusively of information words (see column 9, lines 30-34, type 2 block that includes at least one control word, see figure 4b):

condensing the block to accommodate a TYPE word (see column 9, lines 35-37, the eight-bit field is occupied by the type word and the 56-bit sub-field is occupied by a condensed version of a block, see figure 4c); generating the TYPE word having a value that indicates one of the following structural properties of the block (see column 9, lines 50-59, type word in block 157 as shown in figure 4c):

(a) a position of the start of the packet in the block (see column 9, lines 50-59, the control word S and T position is indicated by the type word included in the subfield 157),

(b) a position of the end of the packet in the block (see column 9, lines 50-59, the control word S and T position is indicated by the type word included in the subfield 157), and

(c) the block being composed exclusively of control words (see column 9, lines 50-59, the control word S and T position is indicated by the type word included in the subfield 157), inserting a TYPE word into the block (see column 9, lines 50-59, type word in block 157 as shown in figure 4c), and appending to the block a two bit block header having a second sense (see figure 4c, bit 151 ), opposite to the first sense, to form the frame (see column 9, lines 30-35, the master transition in the sync field 10).

Walker does not expressly disclose appending to the block a one bit block header having a first sense to form the frame and appending to the block a one bit block header having a second sense, opposite to the first sense, to form the frame.

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Sakoda discloses appending to the block a one bit block header having a first sense to form the frame (see figure 3a, one bit header, see column 6, lines 10-40, lines 57-65, one bit header is immediately added, the header information in the data is "0" therefore indicating a long section of information bits) and appending to the block a one bit block header having a second sense, opposite to the first sense, to form the frame (see figure 3a, one bit header, see column 6, lines 10-40, lines 57-65, one bit header is immediately added, see column 7, lines 1-6, header information changed to "1" indicating a different data type).

Sakoda and Walker are analogous art since they are from the same field of endeavor of encoding and transmitting frames.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to use Sakoda's technique of appending to the block a one bit block header having a first sense to form the frame (see figure 3a, one bit header, see column 6, lines 10-40, lines 57-65, one bit header is immediately added, the header information in the data is "0" therefore indicating a long section of information bits) and appending to the block a one bit block header having a second sense, opposite to the first sense, to form the frame (see figure 3a, one bit header, see column 6, lines 10-40, lines 57-65, one bit header is immediately added, see column 7, lines 1-6, header information changed to "1" indicating a different data type) in Walker's method for coding a packet of information words into frames for transmission (see figure 1,64b encoder, see column 4, lines 27-30, 4 lane bus).

The motivation to combine would have been to have a method and apparatus

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that makes it possible to set another transmission during a communication that is in progress such that a plurality of series data of different and same type can be simultaneously transmitted (see column 12, lines 15-19, Sakoda).

**As per claim 2**, Walker discloses condensing the block includes re-coding ones of the control words using fewer bits (see column 9, lines 42-47, all remaining control words are re-coded).

**As per claim 3**, Walker discloses condensing the block includes removing from the block a control word that indicates one of (a) the start of the packet and (b) the end of packet (see column 9, lines 50-55, the control words omitted from the subfield).

**As per claim 4**, Walker discloses condensing the block includes re-coding remaining ones of the control words using fewer bits (see figure 4c, column 9, lines 35-40, condensed version of the block).

**As per claim 5**, Walker discloses the type word is selected from a set of type words having a specified mutual Hamming distance (see column 9, lines 42-47, all remaining control words are re-coded using seven bit codes chosen to have a mutual hamming distance of four bits).

**As per claim 6**, Walker discloses the type words each consist of T bits (see figure 3d); and the method additionally comprises generating the set of possible bit patterns by a process including (see column 24, lines 39-40, T/2 bit pattern): adopting a (T/2)-bit binary pattern as a first half of a bit pattern in the set of possible bit patterns (see column 24, lines 39-40, T/2 bit pattern), and generating a second half of the bit pattern by duplicating or complementing the first half of the bit pattern depending on a

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bit parity value of the first half of the bit pattern (see column 24, lines 40-45, T/2 bit pattern, generating a second half of the bit pattern by duplicating the first half).

**As per claim 7**, Sakoda discloses wherein a one bit block header in the first sense comprises a 1 (see figure 3a, one bit header, see column 6, lines 10-40, lines 57-65, one bit header is immediately added, see column 7, lines 1-6, header information changed to "1" indicating a different data type) and wherein a one bit block header in the second sense comprises a 0 value (see figure 3a, one bit header, see column 6, lines 10-40, lines 57-65, one bit header is immediately added, the header information in the data is "0" therefore indicating a long section of information bits).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to use Sakoda's technique wherein a one bit block header in the first sense comprises a 1 (see figure 3a, one bit header, see column 6, lines 10-40, lines 57-65, one bit header is immediately added, see column 7, lines 1-6, header information changed to "1" indicating a different data type) and a one bit block header in the second sense comprises a 0 value see figure 3a, one bit header, see column 6, lines 10-40, lines 57-65, one bit header is immediately added, the header information in the data is "0" therefore indicating a long section of information bits) as a modification replaces Walker's two bit header for differentiating between two types of exclusive information words and others (see column 9, lines 10-25, a type 1 block composed exclusively of information words, composed of a two bit field 01 and the payload field, by encoding) in Walker's method for coding a packet of information words into frames for transmission (see figure 1,64b encoder, see column 4, lines 27-30, 4 lane bus).

The motivation to combine would have been to have a method and apparatus that makes it possible to set another transmission during a communication that is in progress such that a plurality of series data of different and same type can be simultaneously transmitted (see column 12, lines 15-19, Sakoda).

**As per claim 8**, Sakoda discloses wherein the method is performed in a conjunction with forward error correction to generate FEC data (see column 9, lines 65-67, viterbi decoding).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to use Sakoda's technique (see column 9, lines 65-67, viterbi decoding) as a modification replaces Walker's two bit header for differentiating between two types of exclusive information words and others (see column 9, lines 10-25, a type 1 block composed exclusively of information words, composed of a two bit field 01 and the payload field, by encoding) in Walker's method for coding a packet of information words into frames for transmission (see figure 1,64b encoder, see column 4, lines 27-30, 4 lane bus).

The motivation to combine would have been to have a method and apparatus that makes it possible to set another transmission during a communication that is in progress such that a plurality of series data of different and same type can be simultaneously transmitted (see column 12, lines 15-19, Sakoda).

**As per claim 9**, Walker discloses wherein the method is utilized in a 10 gigabit/second communication system (see column 6, line 13, 10 Gb/s Ethernet standard).

**As per claim 10**, Walker discloses for the frame transmission over twisted pair conductor (see figure 1, 64b encoder, see column 4, lines 27-30, 4 lane bus).

**As per claim 11**, Walker discloses an apparatus for coding of blocks of input data into respective frames for transmission (see figure 1, 64b encoder, see column 4, lines 27-30, 4 lane bus), the input data including control words and a packet of information words (see column 7, lines 1-10, composed of information words and control words), the packet having (a) a start preceded by ones of the control words and (b) an ending followed by others of the control words (see figure 2, SOP 131 and EOP 132, see column 7, lines 10-21, the control words in the four lanes the start of the packet indicated by SOP control word S, then information words, followed by EOP control word T), the blocks being smaller than the packet (see column 7, lines 1-10, data received by encoder 100 via the four lanes of the bus, composed of information words and control words, the number of information words in the packet 130 is substantially fewer than the minimum number of information words in an Ethernet packet), the frames including a frame corresponding to the packet (see figure 4a-4c, bits, information bits, type, control), the apparatus comprising:

a type word generator configured to (a) receive the block and (b) generate a TYPE word for the block (see figure 8a, type word generator 181 ), the TYPE word having a value that indicates one of the following structural properties of the block (see column 9, lines 50-59, type word in block 157 as shown in figure 4c):

(a) whether the block is composed exclusively of control words (see figure 7b, Z is control word, see figure 3b, control only, see column 8, lines 12-15, the block from

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which the frame is derived is composed exclusively of control words),

(b) a position of the start of the packet in the block (see column 9, lines 50-59, the control word S and T position is indicated by the type word included in the subfield 157),

(c) a position of the end of the packet in the block (see column 9, lines 50-59, the control word S and T position is indicated by the type word included in the subfield 157), and

a two bit block header generator configured to (a) generate a two bit block header in a first sense when the TYPE word indicates that the block is composed exclusively of information words (see column 9, lines 10-25, a type 1 block composed exclusively of information words, composed of a two bit field 01 and the payload field, by encoding), and (b) otherwise generates the two bit block header in a second sense, opposite to the first sense (see column 9, lines 30-34, type 2 block that includes at least one control word, see figure 4b);

a payload field generator (see figure 8a, pay-load field generator 182) configured to adopt the block to form a payload field of the frame when it is determined that the block is composed exclusively of information words (see column 16, lines 10-16, the payload generator operates in response to the type word, when the type word indicates that the block is composed exclusively of information words, it adopts a block to form a payload field), and (b) condense the block and insert the TYPE word into the block to form the payload field when it is determined that the block is not composed exclusively of information words (see column 16, lines 10-16, otherwise condenses the block and



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inserts the type word into the block to form the payload field); and

a frame assembler that appends the block header to the payload field to form the frame (see figure 8a, frame assembler 185, see column 16, lines 43-63, the master transition generator generates the master transition and feeds it to the frame assembler which appends the master transition to the payload to form the frame for transmission).

Walker does not expressly disclose a one bit block header generator that generates a one bit block header in a first sense and one bit block header in a second sense, opposite to the first sense.

Sakoda discloses a one bit block header generator that generates a one bit block header in a first sense (see figure 3a, one bit header, see column 6, lines 10-40, lines 57-65, one bit header is immediately added, the header information in the data is "0" therefore indicating a long section of information bits) and one bit block header in a second sense, opposite to the first sense (see figure 3a, one bit header, see column 6, lines 10-40, lines 57-65, one bit header is immediately added, see column 7, lines 1-6, header information changed to "1" indicating a different data type).

Sakoda and Walker are analogous art since they are from the same field of endeavor of encoding and transmitting frames.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to use Sakoda's technique of a one bit block header generator that generates a one bit block header in a first sense (see figure 3a, one bit header, see column 6, lines 10-40, lines 57-65, one bit header is immediately added, the header information in the data is "0" therefore indicating a long section of information bits) and one bit block

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header in a second sense, opposite to the first sense (see figure 3a, one bit header, see column 6, lines 10-40, lines 57-65, one bit header is immediately added, see column 7, lines 1-6, header information changed to "1" indicating a different data type) as a modification that replaces Walker's two bit header for differentiating between two types of exclusive information words and others (see column 9, lines 10-25, a type 1 block composed exclusively of information words, composed of a two bit field 01 and the payload field, by encoding) in Walker's method for coding a packet of information words into frames for transmission (see figure 1,64b encoder, see column 4, lines 27-30, 4 lane bus).

The motivation to combine would have been to have a method and apparatus that makes it possible to set another transmission during a communication that is in progress such that a plurality of series data of different and same type can be simultaneously transmitted (see column 12, lines 15-19, Sakoda).

**As per claim 12**, Walker discloses the payload field generator includes a re-coder configured to condense the block includes re-coding remaining ones of the control words using fewer bits (see column 9, lines 42-47, all remaining control words are re-coded).

**As per claim 13**, Walker discloses the payload field generator includes a control word removal module configured to condense the block by removing from the block a control word that indicates one of (a) the start of the packet and (b) the end of packet (see column 9, lines 50-55, the control words omitted from the subfield).

**As per claim 14**, Walker discloses the payload field generator includes

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additionally includes a re-coder configured to condense the block includes re-coding remaining ones of the control words using fewer bits (see figure 4c, column 9, lines 35-40, condensed version of the block).

**As per claim 15**, Walker discloses the re-coder to re-code the control words using codes having a specified mutual Hamming distance (see column 9, lines 42-47, all remaining control words are re-coded using seven bit codes chosen to have a mutual hamming distance of four bits).

**As per claim 16**, Walker discloses the type word is selected from a set of type words having a specified mutual Hamming distance (see column 9, lines 42-47, all remaining control words are re-coded using seven bit codes chosen to have a mutual hamming distance of four bits).

**As per claim 17**, Walker discloses the type words each consist of T bits (see figure 3d); the coder additionally comprises a type word generator configured to generate the set of possible bit patterns (see column 24, lines 39-40, T/2 bit pattern): a first-half generator configured for adopting a (T/2)-bit binary pattern as a first half of a bit pattern in the set of possible bit patterns (see column 24, lines 39-40, T/2 bit pattern), and second-half generator configured for generating a second half of the bit pattern by duplicating or complementing the first half of the bit pattern depending on a bit parity value of the first half of the bit pattern (see column 24, lines 40-45, T/2 bit pattern, generating a second half of the bit pattern by duplicating the first half).

**As per claim 18**, Sakoda discloses a forward error correction coder configured to perform with forward error correction coding on a group of two or more frames (see

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column 9, lines 65-67, viterbi decoding).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to use Sakoda's technique (see column 9, lines 65-67, viterbi decoding) as a modification replaces Walker's two bit header for differentiating between two types of exclusive information words and others (see column 9, lines 10-25, a type 1 block composed exclusively of information words, composed of a two bit field 01 and the payload field, by encoding) in Walker's method for coding a packet of information words into frames for transmission (see figure 1,64b encoder, see column 4, lines 27-30, 4 lane bus).

The motivation to combine would have been to have a method and apparatus that makes it possible to set another transmission during a communication that is in progress such that a plurality of series data of different and same type can be simultaneously transmitted (see column 12, lines 15-19, Sakoda).

**As per claim 19**, Walker discloses wherein frame assembler is utilized in a 10 gigabit/second communication system (see column 6, line 13, 10 Gb/s Ethernet standard).

**As per claim 20**, Walker discloses a transceiver configured for the frame transmission and reception over twisted pair conductors (see figure 1,64b encoder, see column 4, lines 27-30, 4 lane bus).

***Conclusion***

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC MYERS whose telephone number is (571)272-0997. The examiner can normally be reached on Monday - Friday 9:30-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Thier can be reached on (571)272-2832. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ERIC MYERS/  
Examiner, Art Unit 2474

/MICHAEL THIER/  
Supervisory Patent Examiner, Art Unit 2474

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**STATEMENT UNDER 37 CFR 3.73(c)**Applicant/Patent Owner: Brett A. McClellanApplication No./Patent No.: 13/925,605 Filed/Issue Date: June 24, 2013Titled: COMMUNICATION SYSTEM AND ENCODING METHOD HAVING LOW OVERHEADMARVELL INTERNATIONAL LTD., a CORPORATION

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1.  The assignee of the entire right, title, and interest.
2.  An assignee of less than the entire right, title, and interest (check applicable box):
- The extent (by percentage) of its ownership interest is \_\_\_\_\_%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3.  The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4.  The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A.  An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel \_\_\_\_\_, Frame \_\_\_\_\_, or for which a copy thereof is attached.
- B.  A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Brett A. McClellan To: Solarflare Communications, Inc.The document was recorded in the United States Patent and Trademark Office at  
Reel 03240018084, Frame 0203, or for which a copy thereof is attached.2. From: Solarflare Communications, Inc. To: Marvell International Ltd.The document was recorded in the United States Patent and Trademark Office at  
Reel 026434, Frame 0922, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**STATEMENT UNDER 37 CFR 3.73(c)**

3. From: Solarflare Communications, Inc. To: Marvell International Ltd.

The document was recorded in the United States Patent and Trademark Office at  
Reel 026434, Frame 0910, or for which a copy thereof is attached.

4. From: \_\_\_\_\_ To: \_\_\_\_\_

The document was recorded in the United States Patent and Trademark Office at  
Reel \_\_\_\_\_, Frame \_\_\_\_\_, or for which a copy thereof is attached.

5. From: \_\_\_\_\_ To: \_\_\_\_\_

The document was recorded in the United States Patent and Trademark Office at  
Reel \_\_\_\_\_, Frame \_\_\_\_\_, or for which a copy thereof is attached.

6. From: \_\_\_\_\_ To: \_\_\_\_\_

The document was recorded in the United States Patent and Trademark Office at  
Reel \_\_\_\_\_, Frame \_\_\_\_\_, or for which a copy thereof is attached.

Additional documents in the chain of title are listed on a supplemental sheet(s).

As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Gregory E. Stanton #45,127/

Signature

Gregory E. Stanton

Printed or Typed Name

September 18, 2014

Date

45,127

Title or Registration Number



## Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.